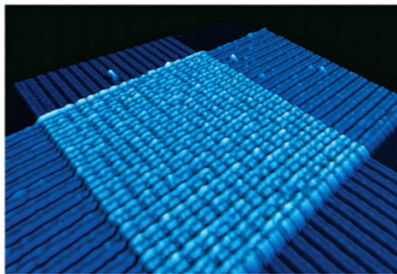


electronic devices and circuit theory

ROBERT L. BOYLESTAD | LOUIS NASHELSKY



eleventh edition

SIGNIFICANT EQUATIONS

1 Semiconductor Diodes $W = QV$, $1 \text{ eV} = 1.6 \times 10^{-19} \text{ J}$, $I_D = I_s (e^{V_D/nV_T} - 1)$, $k = 1.38 \times 10^{-23} \text{ J/K}$, $V_K \cong 0.7 \text{ V (Si)}$, $V_K \cong 0.3 \text{ V (Ge)}$, $V_K \cong 1.2 \text{ V (GaAs)}$, $P_D = V_D I_D$, $T_C = (\Delta V_Z/V_Z)/(T_1 - T_0) \times 100\%/^\circ\text{C}$

2 Diode Applications Silicon: $V_K \cong 0.7 \text{ V}$, germanium: $V_K \cong 0.3 \text{ V}$, GaAs: $V_K \cong 1.2 \text{ V}$, full-wave: $V_{dc} = 0.636 V_m$

3 Bipolar Junction Transistors $I_E = I_C + I_B$, $I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}}$, $I_C = \alpha_{ac} \Delta I_C / \Delta I_E$, $I_{CEO} = I_{CBO} / (1 - \alpha)$, $\beta_{dc} = I_C / I_B$, $\beta_{ac} = \Delta I_C / \Delta I_B$, $\alpha = \beta / (\beta + 1)$, $P_{C_{\text{max}}} = V_{CE} I_C$

4 DC Biasing—BJTs In general: $V_{BE} = 0.7 \text{ V}$, $I_C \cong I_E$, $I_C = \beta I_B$; fixed-bias: $I_{C_{\text{sat}}} = V_{CC} / R_C$; emitter-stabilized: $I_B = (V_{CC} - V_{BE}) / (R_B + (\beta + 1)R_E)$, $R_i = (\beta + 1)R_E \parallel R_B$, $I_{C_{\text{sat}}} = V_{CC} / (R_C + R_E)$; voltage-divider: exact: $R_{Th} = R_1 \parallel R_2$, $E_{Th} = R_2 V_{CC} / (R_1 + R_2)$, $V_{CE} = V_{CC} - I_C(R_C + R_E)$, approximate: $\beta R_E \geq 10 R_2$, $V_B = R_2 V_{CC} / (R_1 + R_2)$, $I_B = (V_{CC} - V_{BE}) / (R_B + \beta(R_C + R_E))$; common-base: $I_B = (V_{EE} - V_{BE}) / R_E$; switch: stability: $S(I_{CO}) = \Delta I_C / \Delta I_{CO}$; fixed-bias: $S(I_{CO}) = \beta + 1$; emitter-bias: $S(I_{CO}) = (\beta + 1)(1 + R_{Th}/R_E) / (1 + \beta + R_{Th}/R_E)$; voltage-divider: $S(I_{CO}) = (\beta + 1)(1 + R_{Th}/R_E) / (1 + \beta + R_{Th}/R_E)$; feedback-bias: $S(I_{CO}) = (\beta + 1)(1 + R_{Th}/R_E) / (1 + \beta + R_{Th}/R_E)$; $S(V_{BE}) = \Delta I_C / \Delta V_{BE}$; fixed-bias: $S(V_{BE}) = -\beta / R_B$; emitter-bias: $S(V_{BE}) = -\beta / (R_B + (1 + \beta)R_E)$; feedback bias: $S(V_{BE}) = -\beta / (R_B + (\beta + 1)R_C)$, $S(\beta) = \Delta I_C / \Delta \beta$; emitter-bias: $S(\beta) = I_{C_1}(1 + R_B/R_E) / (\beta_1(1 + \beta_2 + R_B/R_E))$; voltage-divider: $S(\beta) = I_{C_1}(1 + R_B/R_C) / (\beta_1(1 + \beta_2 + R_B/R_C))$, $\Delta I_C = S(I_{CO}) \Delta I_{CO}$

5 BJT AC Analysis $r_e = 26 \text{ mV} / I_E$; CE fixed-bias: $Z_i \cong \beta r_e$, $Z_o \cong R_C$, $A_v = -R_C / r_e$; CE emitter-bias: $Z_i \cong R_B \parallel \beta R_E$, $Z_o \cong R_C$, $A_v \cong -R_C / R_E$; emitter-follower: common-base: $Z_i \cong R_E \parallel r_e$, $Z_o \cong R_C$, $A_v \cong R_C / r_e$; collector feedback: $Z_i \cong r_e / (1/\beta + R_C/R_E)$; dc feedback: $Z_i \cong R_{F_1} \parallel \beta r_e$, $Z_o \cong R_C \parallel R_{F_2}$, $A_v = -(R_{F_2} \parallel R_C) / r_e$; effect of load impedance: $V_i = R_i V_s / (R_i + R_s)$, $A_{v_s} = R_i A_{v_{NL}} / (R_i + R_s)$, $I_s = V_s / (R_s + R_i)$; impedance: $A_v = R_L A_{v_{NL}} / (R_L + R_o)$, $A_{v_s} = (R_i / (R_i + R_s))(R_L / (R_L + R_o)) A_{v_{NL}}$, $A_i = I_L / I_s$; connection: $A_v = A_{v_1} A_{v_2}$; Darlington connection: $\beta_D = \beta_1 \beta_2$; emitter-follower configuration: $I_C \cong I_E \cong \beta_D I_B$, $Z_i = R_B \parallel \beta_1 \beta_2 R_E$, $A_i = \beta_D R_B / (R_B + \beta_D R_E)$, $A_v \cong 1$, $Z_o = r_e / \beta_2$

14 Feedback and Oscillator Circuits $A_c = A/(1 + \beta A)$; series feedback: $Z_{ic} = Z_i(1 + \beta A)$

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To Else Marie, Alison and Mark, Eric and Rachel, Stacey and J
and our eight granddaughters: Kelcy, Morgan, Codie, Samantha,
Britt, Skylar, and Aspen.

To Katrin, Kira and Thomas, Larren and Patricia, and our six gr
Justin, Brendan, Owen, Tyler, Colin, and Dillon.

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The preparation of the preface for the 11th edition resulted in a bit of reflection on the years since the first edition was published in 1972 by two young educators. Although we prefer the term *semiconductor* devices rather than *electronic* devices, the first edition was almost exclusively a survey of vacuum-tube devices—a subject without a single entry in the new Table of Contents. The change from tubes to predominantly semiconductor devices took almost five editions, but today it is simply referenced in some sections. Interestingly, however, that when field-effect transistor (FET) devices surfaced in earnest, many of the analysis techniques used for tubes could be applied because of the similar physical and equivalent models of each device.

We are often asked about the revision process and how the content of a new edition is defined. In some cases, it is quite obvious that the computer software has been updated and the changes in application of the packages must be spelled out in detail. This text was the first to emphasize the use of computer software packages and provide a level of detail unavailable in other texts. With each new version of a software package, we have found that the supporting literature may still be in production, or the need for more detail for new users of these packages. Sufficient detail in this text enables the student can apply each of the software packages covered without additional material.

The next requirement with any new edition is the need to update the content to reflect changes in the available devices and in the characteristics of commercial devices. This can require extensive research in each area, followed by decisions regarding the scope of coverage and whether the listed improvements in response are valid and desirable. The classroom experience is probably one of the most important reasons for defining areas that need expansion, deletion, or revision. The feedback from students results in marked up copies of our texts with inserts creating a much-improved

the last edition. When you consider the number along with the length of the text material, this was error-free as possible. Any contributions from us, and the sources were thanked for taking the publisher and to us.

Although the current edition now reflects all the expect that a revised edition will be required some respond to this edition so that we can start developing will help us improve the content for the next edition comments, whether positive or negative.

NEW TO THIS EDITION

- Throughout the chapters, there are extensive changes. New problems have been added, and a significant number of the existing problems.
- A significant number of computer programs were added to include the effects of using OrCAD version 1. In addition, the introductory chapters are now assuming the methods, resulting in a revised introduction to the
- Throughout the text, photos and biographies of individuals. Included among these are Sidney Darlington, V. Colpitts, and Ralph Hartley.
- New sections were added throughout the text. Topics of combined dc and ac sources on diode networks and UMOS power FETs, Early voltage, frequency effect of R_S on an amplifier's frequency response, and a number of other topics.
- A number of sections were completely rewritten, reflecting changing priorities. Some of the areas revised include sources, feedback in the dc and ac modes, miller response, transition and diffusion capacitive effects, characteristics, reverse-saturation current, breakdown, and the hybrid model.
- In addition to the revision of numerous sections, several sections that have been expanded to respond to the kind. The section on solar cells now includes a new employed, additional response curves, and a new coverage of the Darlington effect was totally revised. An examination of the emitter-follower and collector

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PowerPoint Presentation—(ISBN 0132783746). This supplement contains from the text as well as a new set of lecture notes highlighting important conc

TestGen® Computerized Test Bank—(ISBN 013278372X). This electronic questions can be used to develop customized quizzes, tests, and/or exams.

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STUDENT SUPPLEMENTS

Laboratory Manual—(ISBN 0132622459) . This supplement contains over 35 experiments for students to use to demonstrate their comprehension of course

Companion Website—Student study resources are available at www.pearson.com/boylestad

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